A New "Active" Predistorter With High Gain and Programmable Gain and Phase Characteristics Using Cascode-FET Structures

Junghyun Kim, *Student Member, IEEE*, Moon-Suk Jeon, Jaehak Lee, and Youngwoo Kwon, *Member, IEEE*

***Abstract*—A monolithic-microwave integrated-circuit (MMIC)-compatible miniaturized "active" predistorter using cascode FET structures is presented. The predistorter has added functionality of gain, as well as programmable gain and phase variation characteristics, which are required to compensate for the nonlinear distortion of a wide range of power amplifiers (PAs). Thanks to the inherent gain of the predistorter, a need for an additional buffer amplifier is eliminated. Furthermore, it can eventually replace the first-stage amplifier in the multistage PAs, making this approach well suited to MMIC implementation. A simple analysis is performed to understand the phase variation mechanisms in the proposed predistorter and to identify the dominant sources of phase variation. From the analysis, the origins of nonlinear distortion of predistorter were found to be G_m of the upper FET and $R_{\rm ds}$ of the lower FET. It was also found from the analysis that the gain and phase variation can be programmed by controlling the bias and size of the transistors. To demonstrate the general usefulness of this predistorter, the cascode predistorter was applied to linearize watt-level MMIC amplifiers for code-division multiple-access handset applications, as well as 30-W high power amplifiers (HPAs) for base-station applications. Adjacent channel power ratio (ACPR) improvement of 3–5 dB was achieved with off-chip predistorter when applied to 0.9-W monolithic amplifiers. The predistorter was also integrated with a 1.6-W MMIC PA on a single chip, replacing the first-stage transistor of the amplifier. An integrated predistorter showed ACPR improvement of 2.5 dB at 28-dBm output power. When applied to a base-station HPA, the spectral regrowth is suppressed by approximately 10 dB at the average output power of 44.7 dBm. The "active" predistorter of this study can be a viable general-purpose linearization technique that can be applied to a wide range of amplifiers.**

***Index Terms*—Distortion, linearization, monolithic microwave integrated circuit (MMIC), nonlinear, power amplifier (PA), predistorter.**

I. Introduction

A HIGH-EFFICIENCY and high-linearity power amplifier (PA) is a key component for modern communication systems employing complex digital modulation schemes such as code division multiple access (CDMA). To achieve high efficiency, the amplifiers are generally biased at class B or AB, which guarantees low quiescent dc current. However, these reduced-angle bias schemes inevitably result in nonnegligible nonlinear distortions in both AM–AM and AM–PM characteristics. Among the two distortion mechanisms, phase distortion is hard to predict, and has been the topic of extensive research [1]–[3]. Due to the excessive distortions at full power levels, conventional PAs with low quiescent current are usually operated at reduced power levels (called "power backoff") to satisfy the stringent linearity requirement.

Power backoff is, however, inevitably accompanied by severe loss in efficiency. In order to combat this problem, a linearizer is introduced so that the efficiency may not be compromised for linearity. The amount of power backoff can be reduced by employing the linearizers, resulting in enhanced efficiencies [4], [5]. Among various linearization techniques, predistortion is the simplest to implement and can be realized in a small die area [4]–[9], making it most compatible with monolithic-microwave integrated-circuit (MMIC) implementation [4], [8], [9]. A predistortion technique can also be applied for base-station amplifiers [10]. Compared with more complex and sophisticated linearization techniques, such as feed forward [11], the predistortion method provides compromised linearity enhancement, but offers the advantages of low power consumption and simple circuit configurations [12], [13]. The reported predistorters were, however, "passive" and resulted in the insertion losses ranging from several decibels to over 10 dB. A buffer amplifier is thus needed after the predistorter to compensate for the loss, which makes the predistortion system complicated and less attractive for monolithic applications.

In this paper, a new "active" predistorter is proposed using cascode FET structures. The proposed predistorter provides gain, while compensating for both gain and phase distortion. The need for additional buffer amplifiers is eliminated in this way. Moreover, it can eventually replace the first-stage amplifier of the multistage PA, making it highly suited to MMIC implementation.

A simple analysis on the phase characteristics is given in Section II to understand the phase-correction mechanisms of the cascode structure, as well as to identify the dominant sources of phase variation. It is also shown that depending on the biases, the predistorter of this study can be programmed to compensate for phase distortion with both positive and negative slopes, which is a very useful feature as a general-purpose predistorter. In order to demonstrate the usefulness of the proposed predistorter for handset applications, two CDMA MMIC amplifiers employing O-QPSK modulation schemes with 0.9- and 1.6-W output power levels have been linearized with an off- and on-chip "active" predistorter of this study, respectively.

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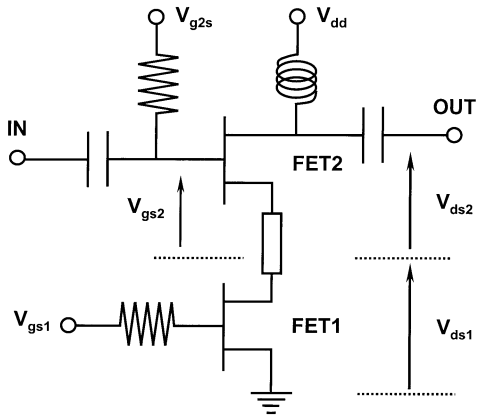


Fig. 1. Configuration of predistorter proposed in this paper.

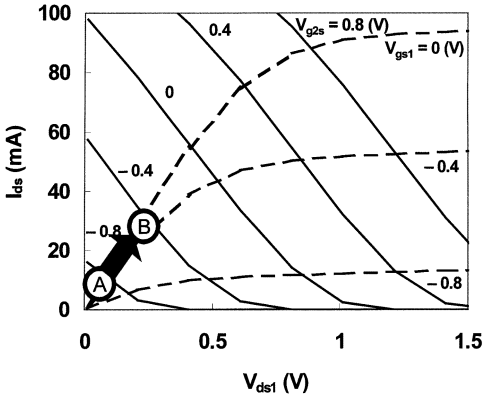


Fig. 2. *I–V* curve of FET1 at each $V_{\rm gs1}$ and $V_{\rm g2s}$ bias voltage.

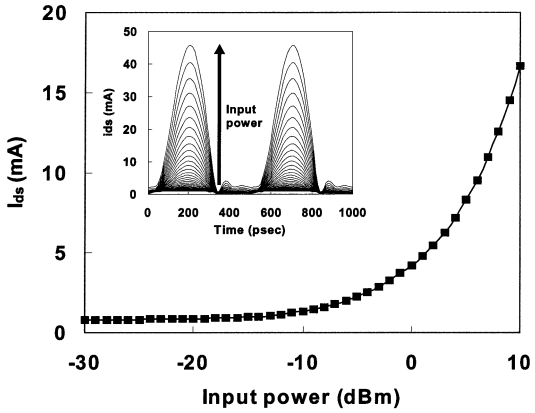


Fig. 3. DC component of the rectified current. Also shown in the inset is the time-domain waveform of RF current according to input power level.

In addition, the predistorter was also applied to linearize 30-W-level CDMA base-station amplifiers that employ a different modulation scheme, i.e., QPSK. The improvement in adjacent channel power ratio (ACPR) was 2–5 dB in handset amplifiers and as much as 10 dB for base-station amplifiers. Detailed measured results are presented in Section III.

II. Design Concept and Analysis

Typically, a PA shows gain compression and unpredictable phase deviation at high power levels. Thus, the predistorter is required to present positive gain and compensatory phase slopes at high power levels. Fig. 1 is the configuration of predistorter proposed in this paper. It consists of two FETs connected in a cascode configuration, and bias inductors and resistors. It is simple and can be implemented easily in MMIC forms.

The input is connected to the gate of the upper FET (FET2), and the output is taken from the drain of the same FET. Hence, the power gain can be obtained from this predistorter. The lower FET (FET1) operates as a degenerating nonlinear load to the upper FET (FET2), as well as a device to set the bias of the upper FET depending on the input power levels. Due to the fact that both FETs of the cascode structure share the same current path, and $V_{\rm dd}$ voltage is divided between the two FETs, it is possible to change the effective bias point of the FET2 with the input power levels, as illustrated in Fig. 2. Fig. 2 is the *I–V* curve of FET1 at each $V_{\rm gs1}$ and $V_{\rm g2s}$ bias voltage. Depending on the biases to each transistor, the various mode of operation can be obtained, as will be shown below. In the basic mode of operation, the "A region" is selected as the standby bias point, which guarantees very small standby current, resulting in negligible dc power consumption. As the input RF power is increased, the dc component of the rectified current increases because the current is clipped from the lower side, as shown in Fig. 3. Therefore, the effective bias point shifts to a higher current region (the "B region" in Fig. 2) at high power levels. Since the effective bias current to the FET2 is increased, the gain becomes higher, resulting in positive gain slope. More detailed design description and analysis is followed.

A. Analysis Algorithm

Unlike the gain characteristics, it is hard to predict and understand the phase variation as a function of input power levels [1]–[3]. The goal of this analysis is to understand the phase-distortion mechanisms in the proposed predistorter and to identify the dominant sources of phase distortion, and finally, based on such information, to come up with a design method to control the phase and gain characteristics as required for linearization. For this purpose, a custom computer program to analyze the phase distortion mechanisms in the cascode-connected FET structure has been developed on the basis of a time-varying harmonic-balance method. First, the predistorter was replaced by a cascode connection of two single-gate FETs, and the equivalent circuit of each transistor was reduced to simplify the analysis. Fig. 4 shows the simplified equivalent-circuit schematic of a predistorter. The FET1 is approximated by a parallel combination of a resistor and capacitor ($r_{\rm ds1}$ and $c_{\rm ds1}$), while the FET2 is represented by the equivalent circuit composed of $g_{m2}, r_{\rm ds2}, r_{i2}, c_{\rm ds2}$, and $c_{\rm gs2}$.

The analysis procedure can be summarized as follows. The simple flowchart of the analysis program is shown in Fig. 5. A table-based nonlinear transistor model was extracted from measured multiple-bias S-parameter data. Single-tone harmonic-balance analysis was followed at various input power levels to determine the instantaneous time-domain voltage waveforms at each terminal of the FETs. A commercial harmonic-balance simulator was used for this purpose. Once the instantaneous time-domain voltage waveforms at FET1 and FET2 are found, each nonlinear parameter, i.e., $g_{m2}(v_{\rm gs2}, v_{\rm ds2})$, $r_{\rm ds2}(v_{\rm gs2}, v_{\rm ds2})$, $r_{i2}(v_{\rm gs2}, v_{\rm ds2})$, $c_{\rm ds2}(v_{\rm gs2}, v_{\rm ds2})$, $c_{\rm gs2}(v_{\rm gs2},$

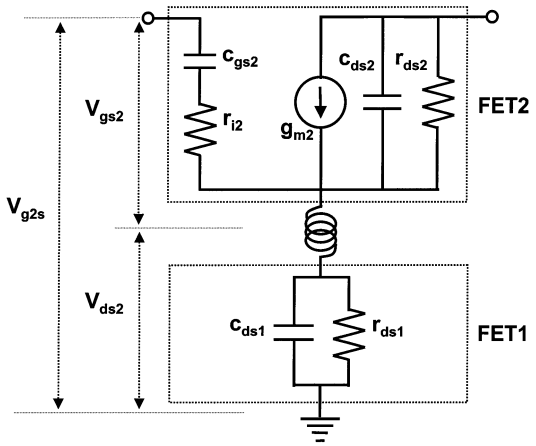


Fig. 4. Reduced equivalent-circuit schematic of a predistorter, as represented by the cascode connection.

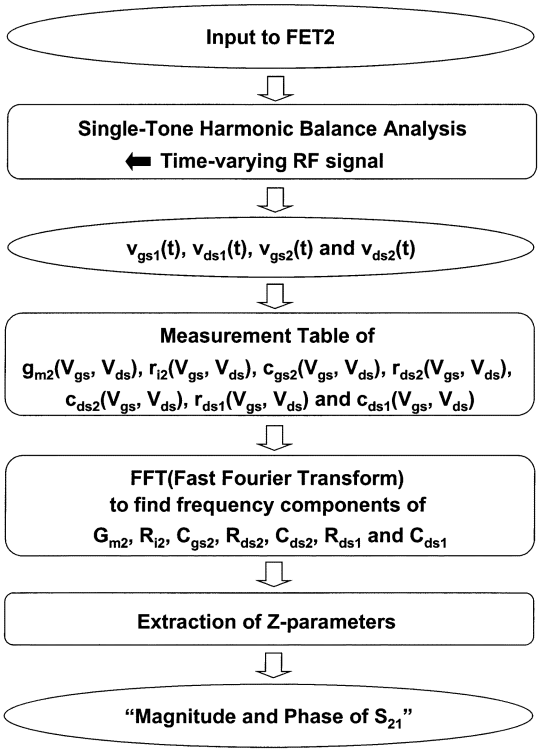
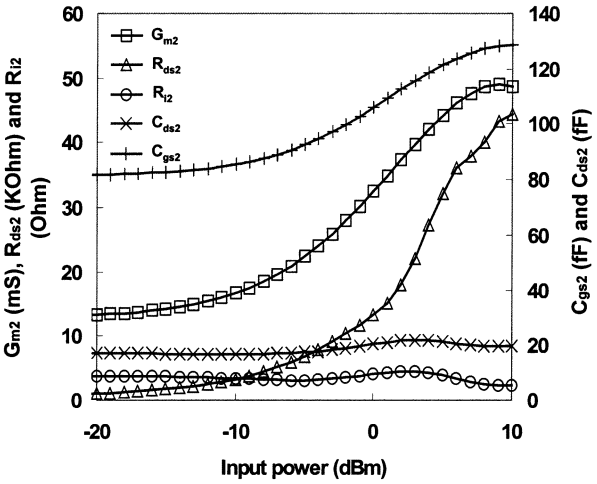
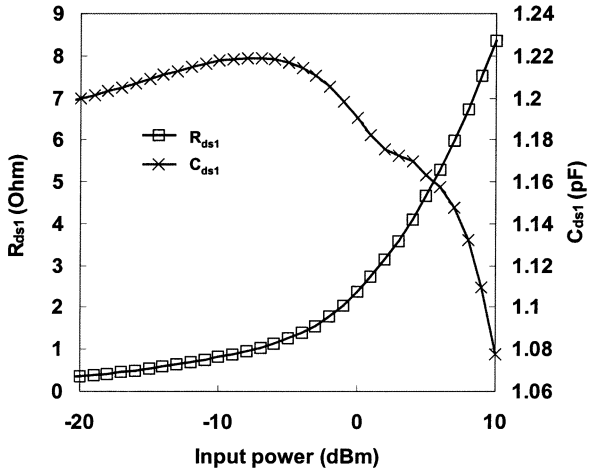


Fig. 5. Flowchart of the analysis program.



(a)



(b)

Fig. 6. Nonlinear parameters in: (a) the upper FET (FET2) and (b) the lower one (FET1) at $V_{\rm gs1}$ of -0.2 V and $V_{\rm g2s}$ of -0.8 V as a function of input power level.

$v_{\rm ds2})$, $r_{\rm ds1}(v_{\rm gs1}, v_{\rm ds1})$, and $c_{\rm ds1}(v_{\rm gs1}, v_{\rm ds1})$, can be expressed in the time domain using the quasi-static model equations of the table-based transistor model.

Fast Fourier transform (FFT) was then performed to find harmonic frequency components of each nonlinear parameter. Fig. 6 shows the fundamental harmonic frequency components of the nonlinear elements as a function of the input power when the transistor was biased in the "A region" ($V_{\rm gs1} = -0.2$ V, $V_{\rm g2s} = -0.8$ V). Fig. 6(a) shows five nonlinear parameters in the FET2, while Fig. 6(b) shows two parameters of the FET1. In order to understand the transfer characteristics of the predistorter, large-signal S_{21}'s of the predistorter are evaluated at each power level using the fundamental frequency components of the nonlinear elements. This means that higher order mixing effects are excluded in the analysis for simplification. This approximation is valid for the input power levels not too close to the full saturation of the transistors, and applies to the general power levels used for predistortion.

For this purpose, the two-port Z-parameters are first expressed from the equivalent circuit of Fig. 4 as follows:

$$z_{11} = \left\{ R_i + \frac{R_{\rm ds1}}{1+\left(\omega R_{\rm ds1} C_{\rm ds1}\right)^2} \right\} + j\left\{ \omega L - \frac{1}{\omega C_{\rm gs}} - \frac{\omega R_{\rm ds1}^2 C_{\rm ds1}}{1+\left(\omega R_{\rm ds1} C_{\rm ds1}\right)^2} \right\} \tag{1}$$

$$z_{21} = \left\{ \frac{R_{\rm ds1}}{1+\left(\omega R_{\rm ds1} C_{\rm ds1}\right)^2} + \frac{G_m R_{\rm ds2}^2 C_{\rm ds2}}{C_{\rm gs}\left(1+(\omega R_{\rm ds1} C_{\rm ds1})^2\right)} \right\} + j\left\{ \omega L - \frac{\omega R_{\rm ds1}^2 C_{\rm ds1}}{1+\left(\omega R_{\rm ds1} C_{\rm ds1}\right)^2} + \frac{G_m R_{\rm ds2}}{\omega C_{\rm gs}\left(1+(\omega R_{\rm ds2} C_{\rm ds2})^2\right)} \right\} \tag{2}$$

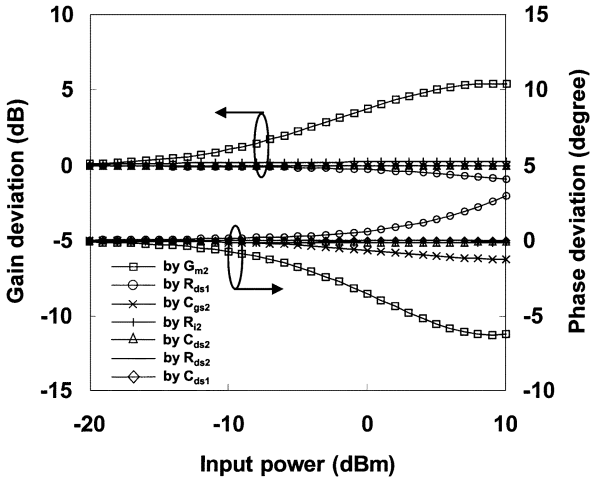


Fig. 7. Effect of each nonlinear parameter on gain and phase variation of the proposed predistorter.

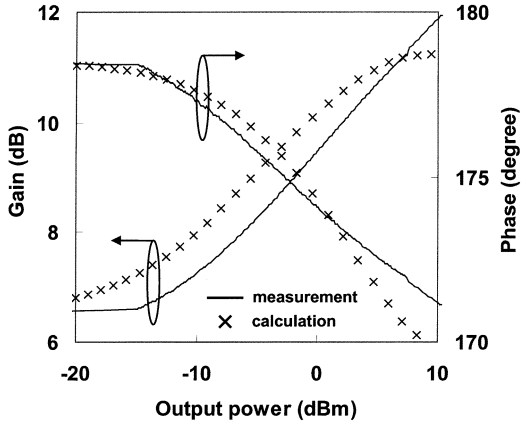


Fig. 8. Measured and calculated gain and phase of predistorter as a function of the output power levels in the basic mode of operation. The biases are fixed at $V_{\rm gs1}$ of -0.2 V and $V_{\rm g2s}$ of -0.8 V.

$$z_{12} = \frac{R_{\rm ds1}}{1+\left(\omega R_{\rm ds1}C_{\rm ds1}\right)^2} + j\left\{\omega L - \frac{\omega R_{\rm ds1}^2 C_{\rm ds1}}{1+\left(\omega R_{\rm ds1}C_{\rm ds1}\right)^2}\right\} \quad (3)$$

$$z_{22} = \left\{\frac{R_{\rm ds1}}{1+(\omega R_{\rm ds1}C_{\rm ds1})^2} + \frac{R_{\rm ds2}}{1+\left(\omega R_{\rm ds2}C_{\rm ds2}\right)^2}\right\} + j\left\{\omega L - \frac{\omega R_{\rm ds1}^2 C_{\rm ds1}}{1+\left(\omega R_{\rm ds1}C_{\rm ds1}\right)^2} - \frac{\omega R_{\rm ds2}^2 C_{\rm ds2}}{1+\left(\omega R_{\rm ds2}C_{\rm ds2}\right)^2}\right\} \quad (4)$$

Two-port Z-parameters are then converted to S_{21} using the following equation:

$$S_{21} = \frac{2Z_{21}Z_0}{\Delta Z} \quad (5)$$

where

$$\Delta Z = (z_{11}+Z_0)(z_{22}+Z_0) - z_{12}z_{21}.$$

Gain (AM–AM) and phase variation (AM–PM) can then be evaluated as a function of the input power. To identify the main sources of AM–AM and AM–PM variation, only a single element is allowed to vary with the power levels, while keeping the other elements constant. Fig. 7 shows the simulated gain and phase variation under this condition. It can be seen that G_m of the FET2 (G_{m2}) and $R_{\rm ds}$ of FET1 ($R_{\rm ds1}$) are most responsible for gain and phase variation in the cascode structure. Also, from Fig. 7, we can easily conclude that the effects of$R_{\rm ds2}, R_{i2}, C_{\rm ds2}, C_{\rm gs2}$, and $C_{\rm ds1}$ on gain and phase deviation are negligible compared to the two major parameters over the entire input power levels. It is also interesting to note that G_{m2} and $R_{\rm ds1}$ have opposite slopes for both gain and phase characteristics. That is, as the input power is increased, gain is expanded and phase is compressed by G_{m2}, while the opposite trends in gain and phase are observed by $R_{\rm ds1}$.

In order to validate the simulation results, a cascode predistorter has been realized in an MMIC form using a 0.15-μm AlGaAs/InGaAs pseudomorphic high electron-mobility transistor (pHEMT) process. Two transistors (FET1 and FET2 in Fig. 1) with a gate periphery of 200 μm have been used in a cascode configuration. Fig. 8 shows the measured and calculated gain and phase of the predistorter as a function of the output power levels in the basic mode of operation; the biases are fixed at $V_{\rm gs1}$ of -0.2 V and $V_{\rm g2s}$ of -0.8 V. Small-signal gain as high as 6.5 dB was obtained together with the required gain and phase predistortion characteristics. The cascode-based predistorter can be effectively used as a first-stage amplifier. Fig. 8 also shows excellent correspondence between the measurement and calculation for both gain and phase characteristics.

B. Programmable Gain/Phase Control Characteristics

Another advantage of the predistorter of this work is the ability to control the gain and phase variation characteristics by changing the biases and size of the transistors. To illustrate the effect of the latter, the size of the transistors has been modified to enhance the range of phase variation. This basic idea comes from the fact that the phase variation due to $R_{\rm ds1}$ and that due to G_{m2} compensates each other at high power levels, as shown in Fig. 7. Therefore, a larger negative phase variation can be obtained if one can minimize the $R_{\rm ds1}$ variation, which is most easily achieved by employing the transistors with larger gate periphery. When the size of the lower transistor is made larger than that of the upper transistor, the $V_{\rm ds}$ swing range of the FET1 is restricted and the instantaneous drain voltage of FET1 remains in the linear region of the *I–V* curve, which results in almost constant $R_{\rm ds1}$. Fig. 9 shows the calculated gain and phase variations for two different gate peripheries of the FET1, i.e., 200 and 400 μm. The size of the FET2 is fixed to 200 μm. As expected, enhanced phase variation was obtained using a larger size transistor in FET1.

The biases are also very useful control parameters that can be used to program the phase and gain characteristics. Aside from the basic mode ($V_{\rm gs1} = -0.2$ V, $V_{\rm g2s} = -0.8$ V), various modes can be achieved by controlling the biases. For example, $V_{\rm g2s}$ (gate bias to the upper common-gate FET) has a strong effect in determining the range of the phase and gain variations. Depending on $V_{\rm g2s}$, gain and phase deviation characteristics can be tuned as shown in Fig. 10, which shows measured and calculated results at various $V_{\rm g2s}$ voltages and power levels. The gate bias of the FET1 is fixed at -0.2 V for this comparison.

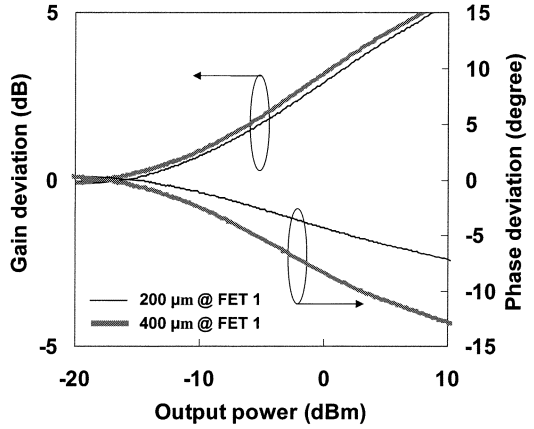


Fig. 9. Calculated gain and phase deviation of predistorter as a function of the output power levels. The lower FET (FET1) with a gate periphery of 400 μm is compared with the one with 200 μm, and gate periphery of the upper FET (FET2) was fixed at 200 μm in both cases.

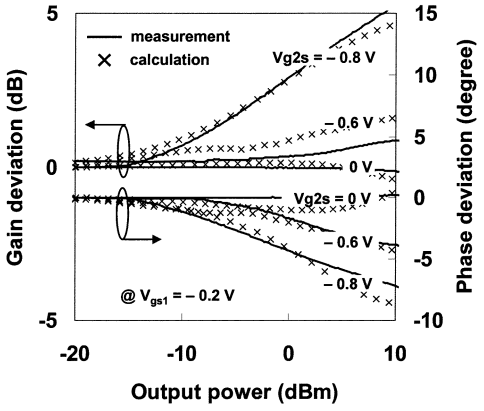


Fig. 10. Measured and calculated gain and phase deviation of predistorter as a function of V_{g2s} and the output power levels at a fixed V_{gs1} of -0.2 V.

One can effectively control the range of the gain and phase variation by simple bias control of V_{g2s}. Fig. 10 also shows very good agreement between simulation and measurement; measured gain was within 1 dB of the calculated and phase was within 2° for most bias conditions. This again validates our simplified analysis method.

PAs sometimes show simultaneous gain and phase compression, i.e., negative phase deviation as the power is increased. This phenomenon, i.e., negative gain and phase slope, can often be developed according to bias conditions, as well as the configuration of the matching circuits including harmonic termination conditions. In order to linearize the PA of this type, the predistorter needs to show the positive gain and phase variations at high power levels. It can be achieved using the predistorter of this study by biasing the FET1 close to the pinchoff, and thereby changing the mode of operation. Measured gain and phase variation of the predistorter is shown in Fig. 11 when the FET1 is biased at V_{gs1} of -0.8 V. Positive phase slope is obtained and the range of the phase overshoot can also be controlled by the V_{g2s} bias. Programming capability of our predistorter is very useful for linearizing a wide variety of the PAs.

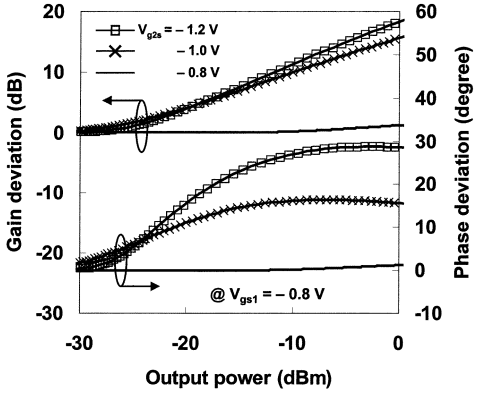


Fig. 11. Measured gain and phase deviation of predistorter as a function of V_{g2s} and the output power levels at a fixed V_{gs1} of -0.8 V.

III. Application to Linearized PA

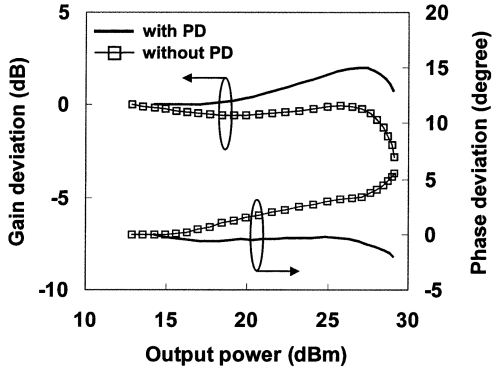
To show the effectiveness of the predistorter of this study for linearizing various PAs, the predistorter has been applied to three different PAs: two watt-level monolithic amplifiers are for CDMA handset applications and one high power amplifier (HPA) is for CDMA base stations. All these amplifiers showed different AM–AM and AM–PM distortion characteristics before linearization.

A. Off-Chip Linearization of 0.9-W MMIC PA

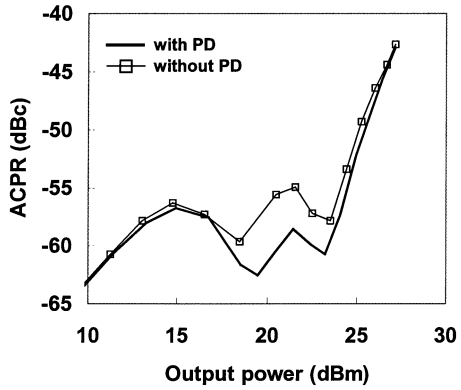
To simply demonstrate the linearizing capability, a cascode predistorter has been implemented on a separate chip and was employed to linearize a three-stage MMIC PA developed for 2-GHz CDMA handset applications. A commercial 0.15-μm AlGaAs/InGaAs pHEMT process was used for the fabrication of a predistorter. The gate periphery for both transistors in a cascode configuration is 200 μm. Total gatewidth of the MMIC PA is 4.8 mm for the power stage, 0.6 mm for the driver stage, and 0.1 mm for the exciter stage.

The MMIC PA was biased at class AB, and showed a linear gain of 33 dB together with a single-tone saturated output power of 29.5 dBm at 2 GHz. This amplifier showed gain compression and phase expansion characteristics, i.e., positive phase deviation (5°) near 1-dB gain compression power level (28 dBm). To compensate for a PA of this type, gain expansion and phase compression is required at high power levels. For this purpose, the predistorter was biased in the A region ($V_{\mathrm{gs1}} = -0.2$ V, $V_{\mathrm{g2s}} = -0.8$ V) of Fig. 2, under which bias the predistorter itself shows a small-signal gain as high as 6.5 dB.

Fig. 12(a) compares the measured gain and phase variation of the PA with and without the predistorter. Phase deviation was reduced to less than 2° over the entire power levels up to the $P_{1\,\mathrm{dB}}$ compression point. Gain degradation at 28-dBm output power was also reduced from 1 to 0.3 dB with the application of the predistorter. Improved AM–AM and AM–PM characteristics enhance the linearity of the amplifier, which is reflected in an ACPR parameter. Fig. 12(b) shows the measured ACPR of the linearized amplifier using O-QPSK CDMA modulated signals. The ACPR was improved by 3 dB at an output power level of 23.5 dBm and 5 dB at 20.5-dBm output power.



(a)



(b)

Fig. 12. Measured: (a) gain and phase deviation and (b) ACPR of the linearized 0.9-W CDMA MMIC PA.

B. 1.6-W-Level Linearized MMIC PA

One of the key advantages of the predistorter of this study is the compatibility with monolithic integration. To demonstrate this, the cascode predistorter has been integrated with a 1.6-W MMIC PA on a single chip. The integrated linearized PA was designed and implemented for Korean personal communications system (K-PCS) handset applications at 1.765 GHz. Moreover, the first stage was replaced by this on-chip predistorter, resulting in three-stage amplifiers including the predistorter. This eliminates the need for additional amplifying stage, resulting in a small die size. A commercial GaAs pHEMT foundry was used for the fabrication. The total gatewidth is 6.4 mm for power stage, 0.8 mm for driver stage, and 200 μm for the two transistors (FET1 and FET2 in Fig. 1) of the predistorter. The photograph of the fabricated MMIC PA with the integrated predistorter is shown in Fig. 13.

The integrated amplifier shows a linear gain of 29 dB and a single-tone saturated output power of 32.5 dBm at 1.765 GHz. Fig. 14(a) shows the measured AM–AM and AM–PM characteristics of the linearized monolithic amplifier. For comparison, a two-stage MMIC PA without a predistorter was also fabricated and the measured results are compared in Fig. 14. It is worthwhile to note that the two-stage MMIC PA without the predistorter shows simultaneous gain and phase compression characteristics, i.e., negative gain and phase deviation at high power levels. Therefore, gain and phase overshoot is required at high power levels. Based on the data shown in Fig. 11, the bias point of predistorter was chosen to be V_{gs1} of -0.8 V and V_{g2s} of

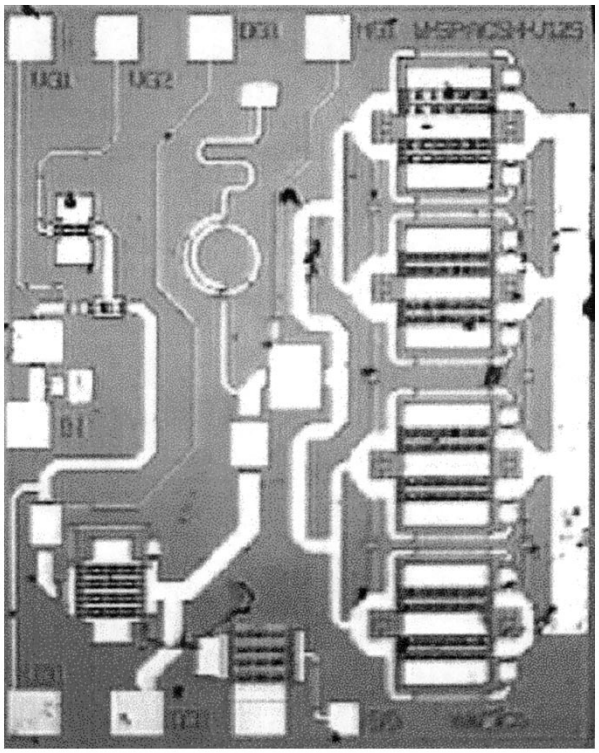
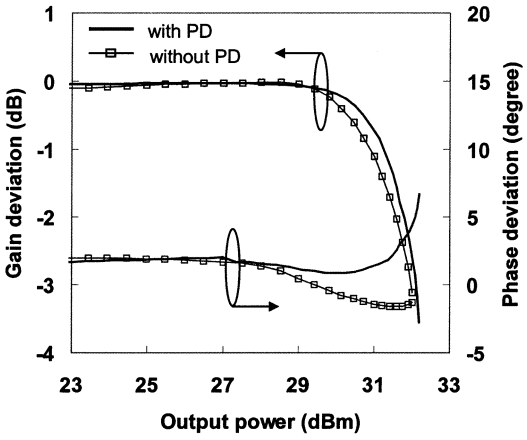
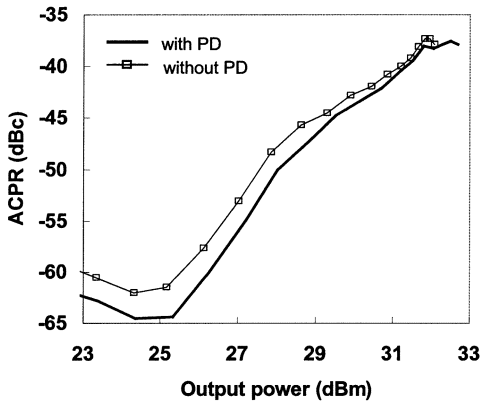


Fig. 13. Fabricated 1.6-W MMIC PA integrated with the predistorter.

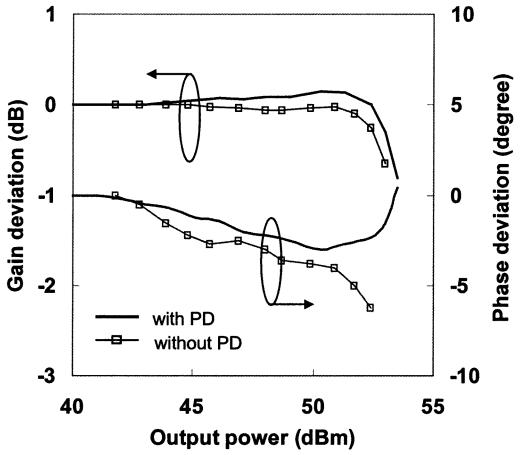


(a)

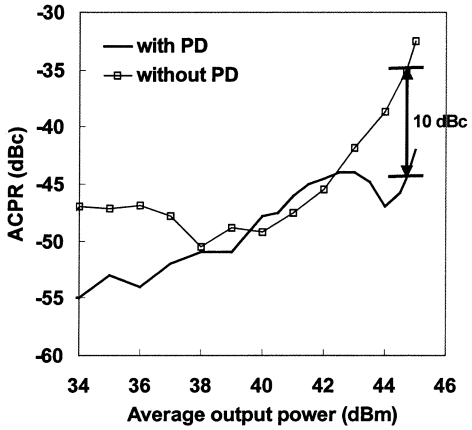


(b)

Fig. 14. Measured: (a) gain and phase deviation and (b) ACPR of the 1.6-W CDMA MMIC PA integrated with the on-chip predistorter.



(a)



(b)

Fig. 15. Measured gain and phase deviation of: (a) the 30-W HPA linearized using the predistorter. (b) ACPR before and after linearization.

−1.0 V. Fig. 14(a) shows that the $P_{1\,\mathrm{dB}}$ compression point of the linearized PA increased from 30.7 to 31.3 dBm. The linearized amplifier also shows reduced phase variation; the phase deviation is decreased to less than 2° for the power levels all the way up to the $P_{1\,\mathrm{dB}}$ compression point. Fig. 14(b) shows the comparison of the ACPR of the amplifiers measured using O-QPSK CDMA modulated signals. Due to the compensated AM–AM and AM–PM characteristics, the ACPR was improved by over 2.5 dB up to the rated output power level of 28 dBm. The ACPR improved from −47.5 to −50 dBc at 28-dBm output power.

C. 30-W-Level Linearized HPA for Base Station

The predistorter of this study was also used to linearize the HPA for base station to demonstrate general adequacy of the proposed approach for PAs with various modulation schemes, and transistors, as well as a wide range of power levels. A 30-W PA has been developed using LDMOS transistors. The modulation scheme used for the CDMA base-station HPA is QPSK, and the center frequency is 1.855 GHz. It consists of two stages. The driver stage uses a 30-W LDMOS FET and the main stage uses two-way combined 125-W LDMOS FETs.

The HPA without a predistorter showed simultaneous gain and phase compression as the amplifier enters the saturation region, as shown in Fig. 15(a). One thing to note is that the phase degradation occurs at the power levels well below the $P_{1\,\mathrm{dB}}$ compression point in this HPA. To compensate for the nonlinearities of this HPA, the predistorter was biased to present gain and phase overshoot at high power levels. Fig. 15(a) illustrates the power-dependent gain and phase characteristics before and after the predistortion. After linearization, $P_{1\,\mathrm{dB}}$ compression point increased from 52.7 to 53.4 dBm, and phase deviation decreased from 7° to 3° for the power levels up to the $P_{1\,\mathrm{dB}}$ compression point. Fig. 15(b) shows the improvement in the ACPR by predistortion. The test CDMA signal is a QPSK-modulated signal with a bandwidth of 1.25 MHz. At the average output power of 44.7 dBm, the spectral regrowth of the linearized HPA is suppressed considerably by approximately 10 dB, i.e., from −34 to −44 dBc, at 883-kHz offset from the center frequency. Fig. 16 shows the spectrum before and after linearization.

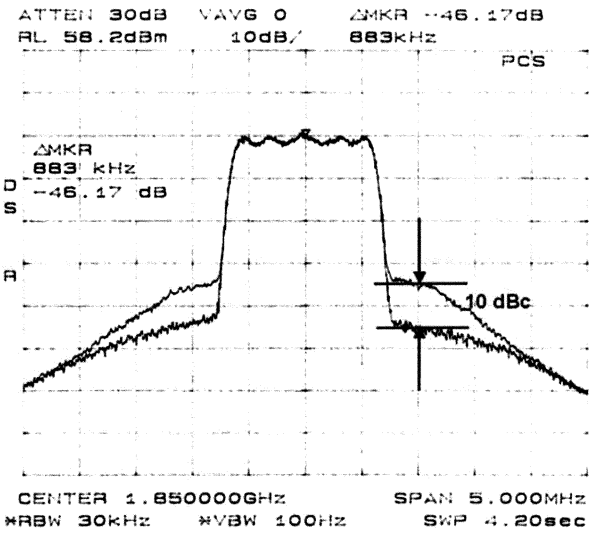


Fig. 16. Spectrum before and after linearization.

IV. Conclusion

A high-gain "active" predistorter using a cascode HEMT structure has been developed. It has shown programmable gain and phase control characteristics so that it may linearize a wide range of PAs. Due to the inherent gain of the predistorter, the need for a buffer amplifier is eliminated, making this approach well suited to MMIC implementation. Moreover, this predistorter can be used as a first amplification stage. A simple analysis has been performed to identify the physical mechanism of the phase and gain variation. From the analysis, the sources of gain and phase variation are found to be G_{m2} and R_{ds1}. The analysis also show that gain and phase variation of the predistorter can be programmed by modifying the power dependence of these two parameters, which is achieved by controlling the bias and size of each transistor.

A predistorter of this study is employed to linearize various amplifiers with different modulation schemes, transistor types, and a wide range of power levels. For CDMA handset PAs using O-QPSK modulation schemes, two types of predistorters were employed for linearization, i.e., off- and on-chip. External off-chip predistorter was used to linearize a 2-GHz 0.9-W

CDMA MMIC PA. It showed the ACPR improvement as high as 3 dB at 23.5-dBm output power and 5 dB at 20.5-dBm output power for O-QPSK signals. The on-chip predistorter was integrated with a 1.6-W CDMA MMIC PA for PCS application, replacing the first-stage amplifier. It also showed the ACPR improvement as much as 2.5 dB at 28-dBm output power for O-QPSK signals. Finally, the predistorter was also used to linearize a 30-W HPA for a CDMA base station. The spectral regrowth of the linearized HPA is suppressed by approximately 10 dB at the average output power of 44.7 dBm. This "active" predistorter provides added functionality of gain to the predistorter, and can be an attractive monolithic linearizer. In addition, due to the programmability of the gain and phase variation, this approach is a viable general-purpose linearization technique that can be applied to a wide range of amplifiers.

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